Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OFFSET N1**
2. **IN –**
3. **IN +**
4. **VCC-**
5. **OFFSET N2**
6. **OUT**
7. **VCC+**

**EX051C**

**MASK**

**REF**

**2 1 7**

**3 4 5 6**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC (or leave Floating)**

**Mask Ref: EX051C**

**APPROVED BY: DK DIE SIZE .044” X .064” DATE: 7/7/16**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: LF411**

**DG 10.1.2**

#### Rev B, 7/19/02